सत्यमेव जयते

INTELLECTUAL PROPERTY **INDIA**

GOVERNMENT OF INDIA
MINISTRY OF COMMERCE & INDUSTRY,
PATENT OFFICE, DELHI BRANCH,
W - 5, WEST PATEL NAGAR,
NEW DELHI - 110 008.

I, the undersigned, being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.* ***994/Del/02*** *dated* ***30th September 2002.***

Witness my hand this 17th Day of September 2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

30 SEP 2002

FORM 1

THE PATENTS ACT, 1970

(39 of 1970)

APPLICATION FOR GRANT OF A PATENT

(See Sections 5(2), 7, 54 and 135)

1. I/we,

STMicroelectronics Pvt. Ltd., an Indian company, of Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India.

2. hereby declare –

(a) that I am/we re in possession of an invention titled ***"An Improved Voltage Level Translator For Translating Low To High Voltage Levels In Digital Intergrated Circuits."***

(b) that the ~~provisional~~/ complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3. further declare that the inventor(s) for the said inventions is/are

(i) ***NARWAL Rajesh, an Indian citizen, of H. No. 955 Sector 6, Karnal, Haryana, India.***

DUPLICATE

4. I/we claim the priority from the application(s) filed in convection countries, particulars of which are as follows: **NA**

5. I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7. That I am/we are the assignee or legal representative of the true and first inventors.

8. That my/our address for service in India is as follows:

ANAND & ANAND, Advocates
B-41, Nizamuddin East
New Delhi – 110 013

Tel Nos.: (11) 4355078, 4355076, 4350360
Fax Nos.: (11) 4354243, 4352060

9- I/We the true and first inventors of this invention or the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.

a) RAJESH,NARWAL an Indian National of H. NO. 955 SECTOR 6 KARNAL HARYANA , INDIA.

Signature

Dated this 30th day of September 2002

10- that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to grant of patent to me/us on this application.

11- Following are the attachment with the application

(a) Complete specification (3 copies)
(b) Abstract
(c) Formal drawings
(d) Power of Attorney
(e) Form 1 (in triplicate)
(f) Form 3 (in duplicate)
(g) Fee Rs. 5000/- In cash/cheque/bank draft bearing no. , date
On Bank.

I/We request that a patent may be granted to me/us for the said invention.

Dated this 30th day of September 2002

Signature
STMicroelectronics Pvt. Limited

To

The Controller of Patents
The Patent Office, Delhi

02-IND-015

Form 2

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THE PATENTS ACT, 1970

COMPLETE SPECIFICATION

SECTION 10

ORIGINAL

'AN IMPROVED VOLTAGE LEVEL TRANSLATOR FOR TRANSLATING LOW TO HIGH VOLTAGE LEVELS IN DIGITAL INTERGRATED CIRCUITS'

STMicroelectronics Pvt. Ltd., *Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed:

AN IMPROVED VOLTAGE LEVEL TRANSLATOR FOR TRANSLATING LOW TO HIGH VOLTAGE LEVELS IN DIGITAL INTERGRATED CIRCUITS

The Field of Invention:

This invention relates to an improved voltage level translator for translating low to high voltage levels in digital intergrated circuits. This invention further relates to an improved method for translating high voltage levels in digital intergrated circuits.

Background of the Invention:

Advances in semiconductor fabrication and manufacturing techniques have led to smaller, denser and more complex integrated circuits. Digital integrated circuits are spearheading the drive to increased densities and smaller geometries. At the same time digital integrated circuits are also being operated at higher speeds. The combination of increased density and higher speeds also results in increased power dissipation, which in turn increases the temperature of the device thereby reducing its reliability. Inorder to counteract the increased power dissipation modern devices are increasingly being designed to operate at reduced voltage levels. Current technology supports digital integrated circuits based on transistors with gate lengths reduced to 0.12u with corresponding supply voltages as low as 1.2V. However the IO requirements of digital integrated circuits are defined by the requirements of external devices and hence remain at voltage levels that are significantly higher than the core circuitry. Typical IO voltages remain at a 3.3 V to 5.0V level while the core circuitry operates at 1.2V. To operate in such an environment it is necessary to use voltage level translators, which translate signals at the lower voltage level of core logic to the higher lower voltage levels of the IO.

A transistor operating at a higher voltage such as 3.3V is designed to have a relatively long gate length to avoid punchthrough. At the same time, the transistor must also have a thicker gate oxide to prevent oxide break down. These transistors are relatively high voltage devices and are termed as 3.3V devices. If a 3.3V device is used for operation at lower voltage levels such as 1.2V, it provides relatively poor performance in term of speed owing to higher channel resistance and higher gate capacitance. In contrast, transistors operating at lower voltage levels are designed with shorter channel lengths to reduce the channel resistance and gate capacitance as the breakdown voltage requirements are lower. The lower resistance and gate capacitance enable significant increase in speed of operation besides providing higher

density. Transistors which are used for lower voltages are low voltage devices and if designed for 1.2V operation are termed as 1.2V devices in the context of this document. Low voltage transistor models are not designed for use with higher voltages because of the risk of punchthrough and gate oxide breakdown.

To exploit the advantages of low voltage core logic and to make it compatible with the high voltage IO interface it is necessary to use a voltage level translator. While there are many techniques used to realize voltage level translators almost all of them produce voltage level translators that do not achieve equal rise and fall time under varying operating conditions resulting in the generation of unwanted glitches and delays.

Modern **FPGAs** utilize core voltages as low as 1.2 volts while IO voltage remains at 3.3 volts. Signals from the 1.2 volt core, if fed directly to circuitry working at higher voltage 3.3 volts will result in unnecessary power dissipation, since the 1.2 volt signal from the core logic will always keep the IO logic's **PMOS** transistor **ON** as its source is connected to 3.3 volts. To overcome this problem it is necessary to incorporate voltage translator circuitry that converts the 1.2 volts signal to 3.3 volts signal without any static power dissipation.

Figure 1 shows a voltage translator according to the prior art as disclosed in **US patent 5,422,523**. In this patent the low voltage input **IN** is fed to the gate of NMOS transistor **104** and also to the gate of a second NMOS transistor **103** through inverter **LV.** Inverter **LV** operates at a low voltage **(VDDL)**. Transistors **103** and **104** are biased through transistors **101** and **102.** The gate of transistor **102** is connected to the output **OUT 1,** while the gate of transistor **101** is connected to node **206.** When **IN** rises from 0 volts to **VDDL**, NMOS transistor **104** is turned-on which reduces the voltage at node **206**. This voltage reduction turns-on PMOS transistor **101** and increases the voltage at **OUT 1**. The output of **LV** at this time is 0 volts which turns-off NMOS transistor **103**. The increase in voltage at **OUT 1** reduces the conduction level of PMOS transistor **102** which further decreases the voltage at **206**. This cycle is repeated until the voltage at **OUT 1** rises to **VDDH**.

Similarly, when **IN** falls from **VDDL** to 0 volts, NMOS transistor **104** turns-off and NMOS transistor **103** turns-on, pulling down **OUT 1** The reduction in voltage at **OUT 1** turns-on PMOS transistor **102** slightly which in turn increases the voltage at node **206**. This condition

decreases the conductivity of **PMOS** transistor **101** leading to further reduction in the voltage at **OUT 1**. This recursive feedback ultimately reduces the voltage at **OUT 1** to 0 volts.

The drawback with this approach is that it is difficult to achieve equal rise fall times under different operating conditions. This difficulty arises from unwanted capacitance effects which become more prominent at low voltages such as 1.2 volts. Also, since the difference between 1.2 volts and 3.3 volts is large the variations of various parameters with operating conditions has a pronounced effect on circuit performance.

The Object and Summary of the Invention:

The object of the invention is to provide a method and device to reliably interface the signals from the core logic to the IO pads when these operate at different voltages.

Another object of the invention is to provide a voltage translator circuit which achieves equal delays and rise fall time under different operation conditions.

It is yet another object of the invention to overcome the disadvantages arising from the bootstrapping of the IO stages.

To achieve these and other objectives this invention provides an improved low voltage to high voltage translator for digital electronic circuits providing reduced rise times, fall times and transition times that remain independent of operating conditions. This is accomplished by modifying a conventional low-to-high voltage translator comprising a first high-voltage switch driven by the input low-voltage signal, a second high-voltage switch driven by the complement of the input low-voltage signal, the output of the first high-voltage switch enabling an active switched load connected to the output of the second high-voltage switch when the first high-voltage switch is OFF and disabling it when the first high-voltage switch is ON, the output of the second high-voltage switch enabling an active switched load connected to the output of the first high-voltage switch when the second high-voltage switch is OFF and disabling it when the second high-voltage switch is ON, the output from the low-to-high voltage translator being provided by the output from the second high-voltage switch to include a switched active pull-up at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the output from the low-to-high-voltage translator and a switched active pull-down at the output of the first high-voltage switch;

controlled by the input low-voltage signal and gated by the complement of the output from the low-to-high-voltage translator, so as at to provide regenerative pull-up and pull-down that also counteracts the bootstrap capacitance at the output of the first high-voltage switch.

Brief Description of the Accompanying Drawings:-

Fig 1 shows a voltage translator according to the prior art.

Fig 2 shows the schematic of a voltage translator in accordance with the present invention.

Fig 3a shows the voltage waveforms of proposed voltage translator.

Fig 3b shows the comparitive bootstraping effect in the prior art and present invention.

Fig 4 shows the simulation waveforms of the prior art circuit as well as the proposed circuit for typical models.

Fig 5 shows the variaton in the simulation waveforms using slow models.

Fig 6 shows the variaton in the simulation waveforms using slowfast models i.e **NMOS** is slow and **PMOS** is fast.

Fig. 7 shows the comparison of waveforms showing the effect of bootstrap capacitance.

Detailed Description:

The invention will now be described in accordance with the accompanying drawings.

Figure 1 has already been described in the background to the invention.

Figure 2 shows a preferred embodiment of the invention. The input **IN** from the core logic is connected to the gates of transistors **N1, P4, N3** and to the gate of NMOS transistor **N2** through inverter **LV1.** Inverter **LV1** is an inverter driven by low voltage. The source of PMOS transistor **P4** is connected to low voltage source (**VDDL**), and the drain is connected to NMOS transistor **N5**. The gate of transistor **N5** is connected to the output **OUT 2,** and the second conducting terminal is connected to line **402.** Voltage source **VDDH** is connected to

the source of PMOS transistors **P1** and **P3.** The gates of the PMOS transistors **P1** and **P3** are cross coupled to drains **402, 404 (OUT 2)** of the NMOS transistors respectively.

The source of NMOS transistor **N1** is connected to **GND** and its drain is connected to line **402**. The gate of transistor **N2** is connected to the output of **LV1**. The source and drain of **N2** are connected to **GND** and **OUT 2** respectively while the conducting terminals of NMOS transistor **N3** are connected to lines **402** and **405**. The source of NMOS transistor **N4** is connected to **GND** and its drain is connected to line **405**. The gate of transistor **N4** is connected to the output of inverter **HV1** through line **407**. OUT2 is connected to the input of inverter **HV1** while the gate of MOS transistor **N5** is connected to **OUT 2**.

When input **IN** is at High voltage (e.g. 1.2 V), PMOS transistor **P4** is OFF and NMOS transistor **N1** is conducting pulling line **402** to **GND**. This makes PMOS transistor **P1** ON. The LOW output of **LV1** turns-off NMOS transistor **N2.** The conduction of PMOS transistor **P1** causes node **OUT 2** to go High. The High voltage (e.g. 3.3V) at **OUT 2** causes inverter **HV1** to make line **407** low thereby turning OFF NMOS transistor **N4** while at the same time turning OFF PMOS transistor **P3** and keeping NMOS transistor **N5** conducting.

When the input **IN** goes from high (1.2V) to low (0V) voltage the gate of NMOS transistor **N1** goes from high to low. The bootstrap capacitance at line **402** takes voltage at this net below 0 volts which delays the process of making **P1** OFF. If slow models are used this delay is increased drastically. **P4** and **N5** are used to overcome this problem. The gate of **N5** is connected to **OUT 2** which is high voltage (3.3V), this keeps **N5** ON. As soon as **IN** goes from high to low, the MOS trnasistor **P4** becomes ON. Because of bootstrapping **N1** tries to take line **402** below 0 volts but the combination of **P4** and **N5** opposes this effect and minimizes the bootstrapping effect. The circuitry tries to balance operation under all operating conditions. **LV1** makes line **406** high voltage (1.2V) which makes NMOS transistor **N2** ON. This reduces voltage at **OUT 2**. Reduction in voltage at **OUT 2** makes PMOS transistor **P3** ON. This further increases the voltage at line **402** thereby making PMOS trnasistor **P1** conduct less thereby reducing voltage at **OUT 2**. As a result, PMOS transistor **P3** turns **ON** harder and this positive feedback ultimately makes **OUT 2** 0 volts. As **OUT 2** becomes 0 volts PMOS transistor **P1** turns fully **OFF** and PMOS transistor **P3** turns fully **ON**. As soon as the falling voltage at **OUT 2** crosses the trip point level of inverter **HV1** line **407** becomes high (3.3V) turning NMOS transistor **N4** ON. NMOS transistor **N3** is

OFF since its gate is connected to **IN** which is 0 volts. In the final stable condition when **IN** and **OUT 2** both are 0 volts there is no conduction path between **VDDH** and **GND** or between **VDDL** and **GND**. Thus there is no static power dissipation in the circuit.

Similarly, when input **IN** makes a transition from low votage to High voltage e.g. 0 volts to 1.2 volts the circuit acts to make **P1** ON as early as possible so that output **OUT 2** reaches **VDDH** volts quickly. When both **IN** and **OUT 2** are at 0V NMOS trnasistor **N5** is OFF and NMOS transistor **N4** is ON. As **IN** increases from 0 volts to 1.2 volts NMOS transistor **N1** and NMOS transistor **N3** start conducting. Since **OUT 2** is still 0 volts inverter **HV1** keeps NMOS transistor **N4** ON. The combination of NMOS trnasistors **N3**, **N4** and **N1** pulls down line **402** to 0 volts faster then the case when there is only **N1** to pull it down. Inverter **LV1** acts to make **N2** OFF. With **P1** begining to conduct the voltage at **OUT 2** starts increasing and as **OUT 2** reaches the trip point of **HV1** the voltage at line **407** reaches 0 volts. This makes NMOS transistor **N4** OFF. The trip point of **HV1** is adjusted according to the amount of time for which NMOS transistor **N4** is to be kept ON. As **OUT 2** starts increasing PMOS trnasistor **P3** starts turning OFF. This will further reduce the voltage at line **402** and ultimately this feedback will take node **OUT 2** to 3.3 volts. This makes PMOS transistor **P3** turn OFF and line **402** becomes 0 volts. In the final stable condition when **IN** is 1.2 volts and **OUT 2** is 3.3 volts there is no conduction path between **VDDH** and **GND** or between **VDDL** and **GND**. Thus there is no static power dissipation in the circuit.

The circuit of this invention compensates for the effect of bootstrapping capacitance and also improves transition times. Low to high transitions are improved by incorporating **N3** and **N4**. **N4** remains **ON** for a very short time just to make **P1 ON** with greater power than if only N1 pulls line **402** down. Thus **N3** and **N4** act only to improve the initial voltage fall at line **402**. Similarly high to low transitions are improved by compensating effects of bootstrapping capacitance. The circuit also works well for converting 3.3V to 5V.

Figure 3a shows voltage waveforms at nodes **IN** and **OUT2** for proposed voltage level translator. The dotted line waveform shows the input waveform at **IN**, while the solid line shows output voltage at node **OUT2**.

Fig 3b shows the voltage waveform at line **402** for an improved voltage level translator according to this invention. The solid line shows voltage at **402** while the dotted line is the waveform at line **402** without using the MOS transistors **N3**, **N4**, **N5** and **P4**. The effect of the

bootstrap capacitor is clearly visible by seeing dotted waveform when voltage at line **402** starts rising. When Input **IN** falls, the voltage at line **402** should rise but because of bootstrapping capacitance the voltage goes below 0 volts. This effect is reduced to a large extent as shown by the solid line waveform. Similarly when **IN** goes from 0 volts to 1.2 volts because of the MOS transistors **N3** and **N4** the initial rate of fall at line **402** becomes faster as shown by the solid line waveform.

Fig 4 shows simulation waveforms of the prior art circuit shown in **Fig 1** and the proposed circuit shown in **Fig 2** along with the input **IN**. **OUT1** and **OUT2** are the voltages at the output node of the prior art and proposed circuits respectively under typical operating conditions. The two waveforms are superimposed and the rise and fall delays are almost the same.

Fig. 5 shows the simulation results when models are changed from typical to slow. The proposed circuit output **OUT2** shows better rise and fall delays and transistion times.

Fig. 6 shows the simulation results when models are changed from typical to slowfast i.e **NMOS** is slow and **PMOS** is fast. The proposed circuit output OUT2 shows better rise and fall delays and transistion times. **NET206** shows the voltage variation at **206** for the prior art circuit of **Fig.1** whereas **NET402** shows the waveform at **402** in the improved circuit of **Fig 2**.

Fig. 7 shows the simulation waveforms at nets **402** and **206** under slowfast models. The waveform clearly shows the reduction in bootstrap effect because of which the voltage rise at **402** is faster. The falling at **402** is also better because of the inclusion of NMOS transistors **N3** and **N4**.

While the foregoing description related to an application comprising 1.2V and 3.3V circuitry, the invention is by no means limited to these operating voltage levels. As any with ordinary skill in the art will realize, the principals employed will work equally well in applications involving other voltage levels. Accordingly, the invention is by no means limited by the foregoing examples but is bounded only by the scope of the claims.

We claim:

1. An improved high voltage to low voltage translator for digital electronic circuits providing reduced rise times, fall times and transition times that remain independent of operating conditions, comprising :
   - a first high-voltage switch driven by the input low-voltage signal,
   - a second high-voltage switch driven by the complement of the input low-voltage signal,
   - the output of the first high-voltage switch enabling an active switched load connected to the output of the second high-voltage switch when the first high-voltage switch is OFF and disabling it when the first high-voltage switch is ON,
   - the output of the second high-voltage switch enabling an active switched load connected to the output of the first high-voltage switch when the second high-voltage switch is OFF and disabling it when the second high-voltage switch is ON,
   - the output from the low-to-high voltage translator being provided by the output from the second high-voltage switch

   characterized in that it includes :
   - a switched active pull-up at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the output from the low-to-high-voltage translator and a switched active pull-down at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the complement of the output from the low-to-high-voltage translator, so at to provide regenerative pull-up and pull-down that also counteracts the bootstrap capacitance at the output of the first high-voltage switch.

2. An improved method for providing high voltage to low voltage translation for digital electronic circuits enabling reduced rise times, fall times and transition times that remain independent of operating conditions, comprising the steps of :
   - providing a first high-voltage switch driven by the input low-voltage signal,
   - providing a second high-voltage switch driven by the complement of the input low-voltage signal,

- causing the output of the first high-voltage switch to enable an active switched load connected to the output of the second high-voltage switch when the first high-voltage switch is OFF and disable it when the first high-voltage switch is ON,
- causing the output of the second high-voltage switch to enable an active switched load connected to the output of the first high-voltage switch when the second high-voltage switch is OFF and disable it when the second high-voltage switch is ON,
- providing the output from the low-to-high voltage translator from the output from the second high-voltage switch

characterized in that it includes :

- providing a switched active pull-up at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the output from the low-to-high-voltage translator and a switched active pull-down at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the complement of the output from the low-to-high-voltage translator, so at to provide regenerative pull-up and pull-down that also counteracts the bootstrap capacitance at the output of the first high-voltage switch.

3. An improved high voltage to low voltage translator for digital electronic circuits providing reduced rise times, fall times and transition times that remain independent of operating conditions substantially as herein described with reference to and as illustrated in figures 2 to 7 of the accompanying drawings.

4. An improved method for providing high voltage to low voltage translation for digital electronic circuits enabling reduced rise times, fall times and transition times that remain independent of operating conditions substantially as herein described with reference to and as illustrated in figures 2 to 7 of the accompanying drawings.

Dated this 30th day of Sept , 2002

Anand

of ANAND & ANAND, Advocates
Agents for the Applicants

ABSTRACT

30 SEP 2002

The invention provides an improved low voltage to high voltage translator for digital electronic circuits providing reduced rise times, fall times and transition times that remain independent of operating conditions. This is accomplished by modifying a conventional low-to-high voltage translator to include a switched active pull-up at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the output from the low-to-high-voltage translator and a switched active pull-down at the output of the first high-voltage switch, controlled by the input low-voltage signal and gated by the complement of the output from the low-to-high-voltage translator, so as at to provide regenerative pull-up and pull-down that also counteracts the bootstrap capacitance at the output of the first high-voltage switch.

ORIGINAL

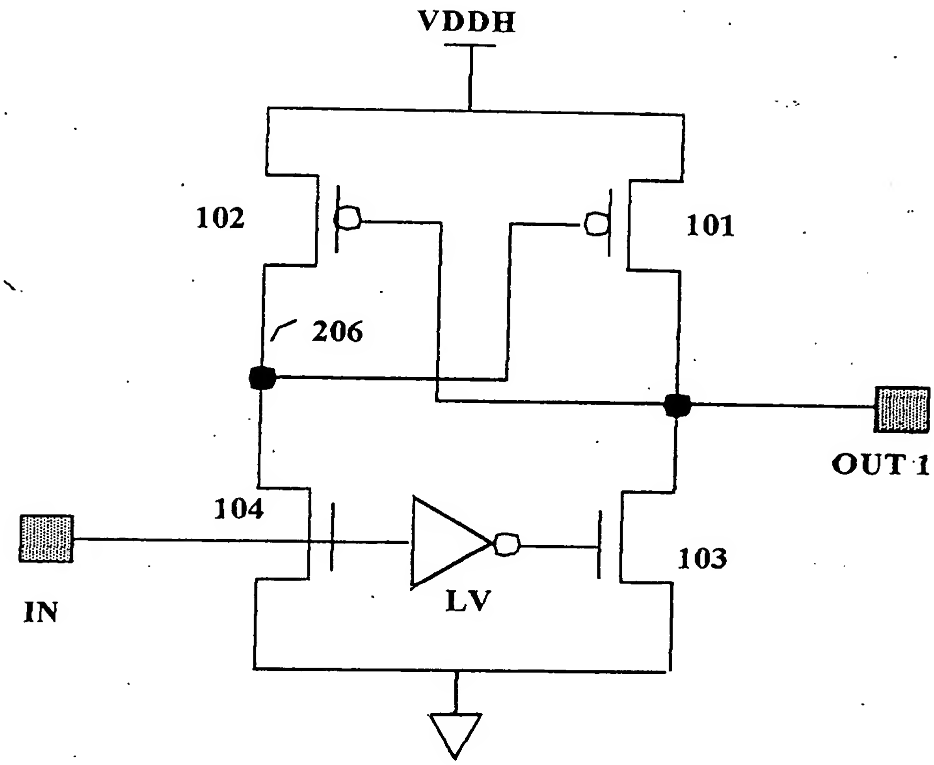

Fig 1

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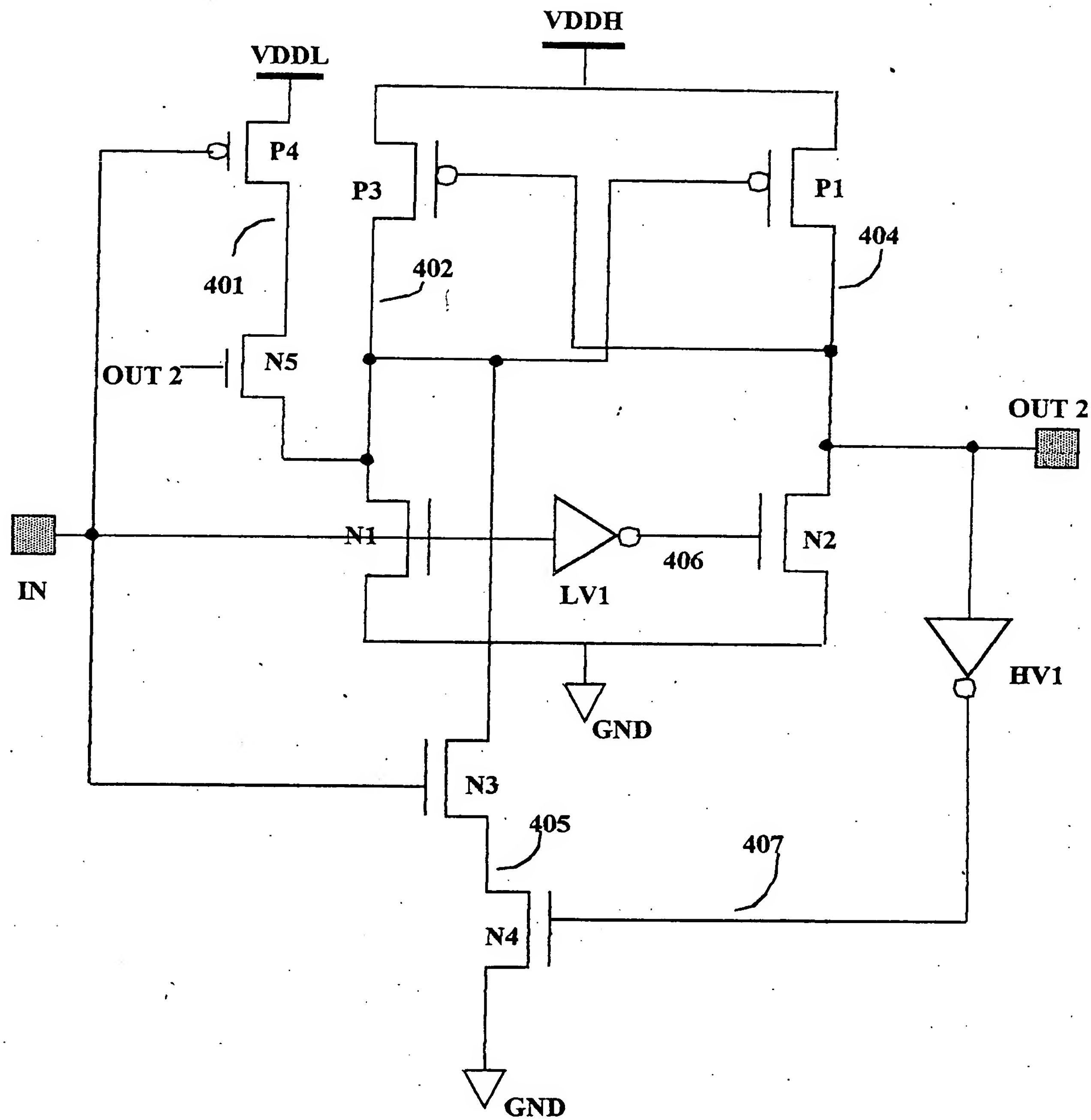

Fig 2

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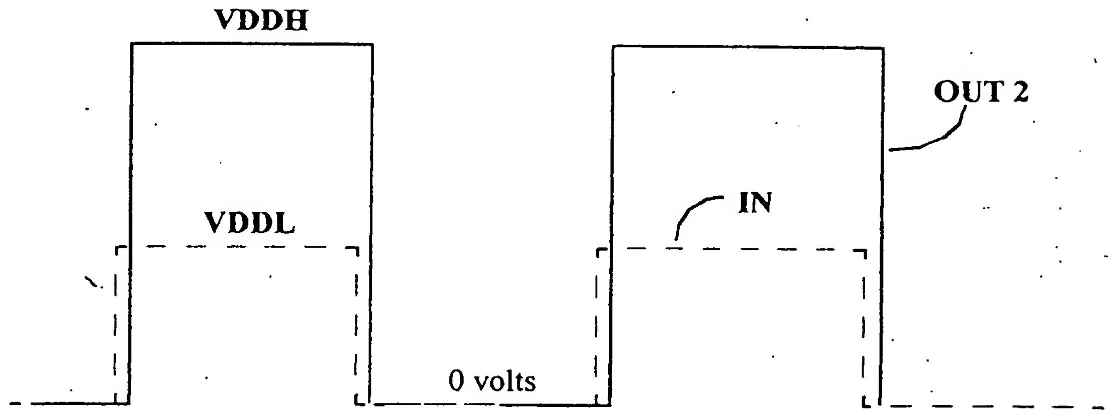

Fig 3a

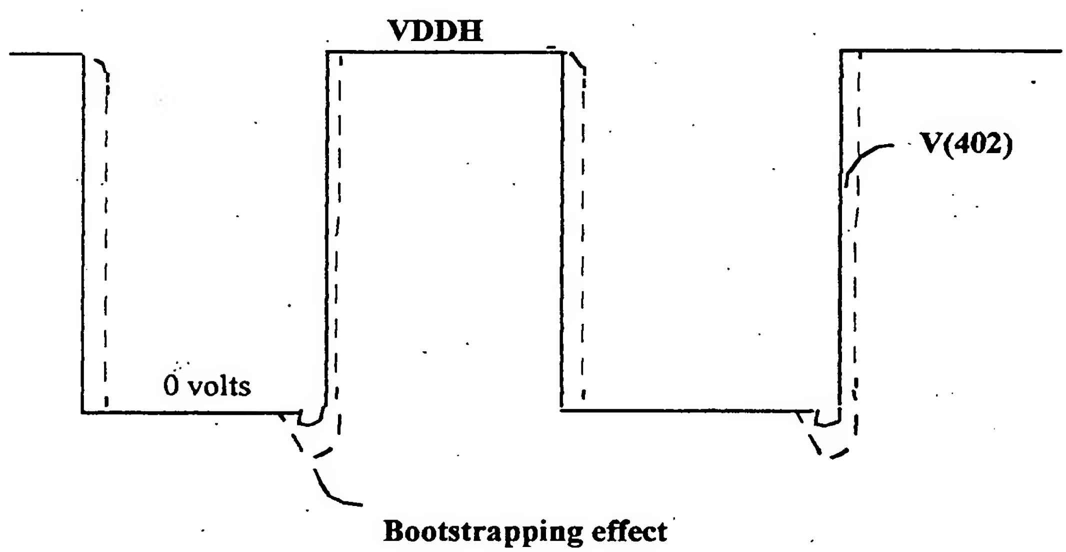

Fig 3b

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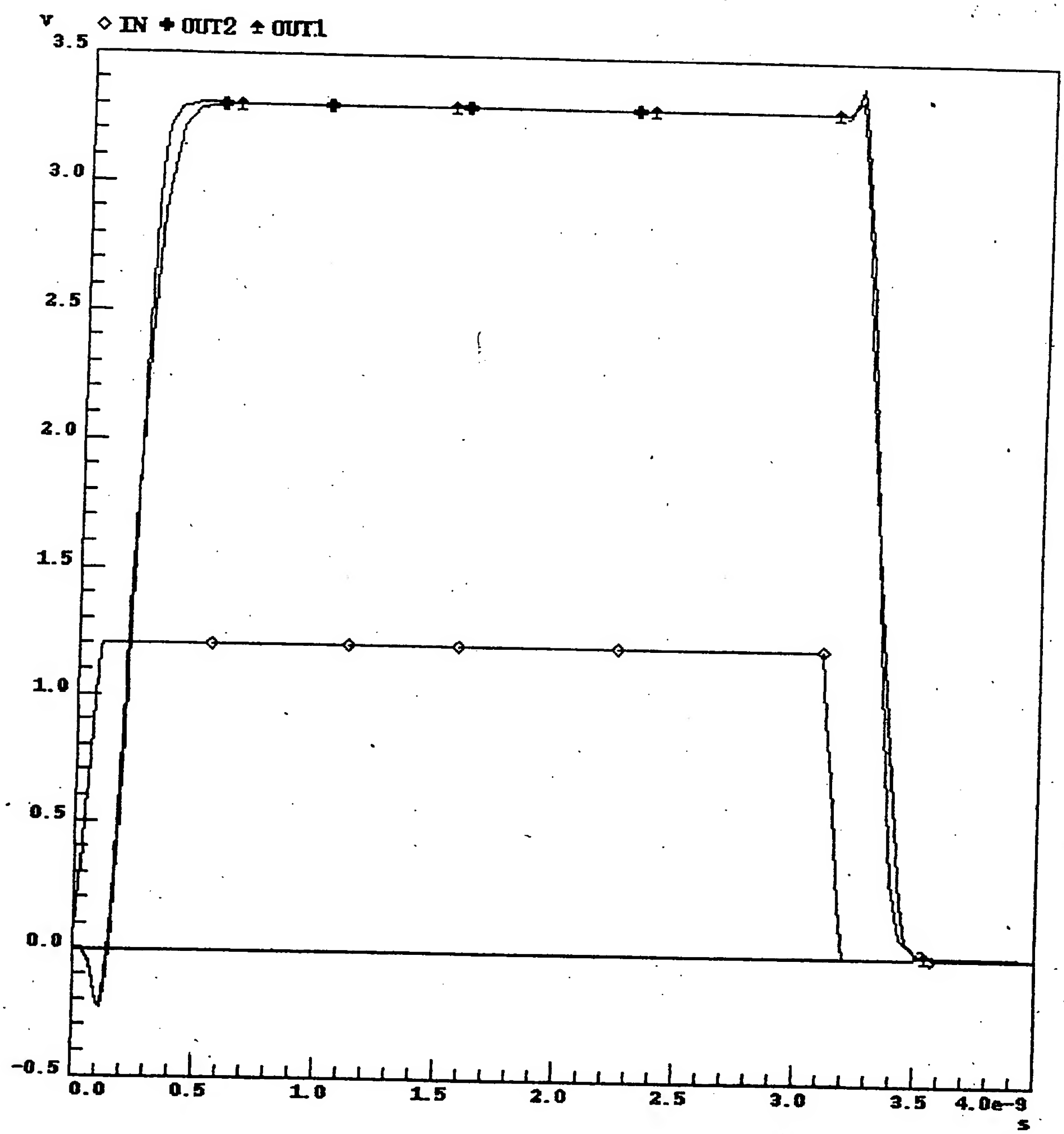

Fig. 4

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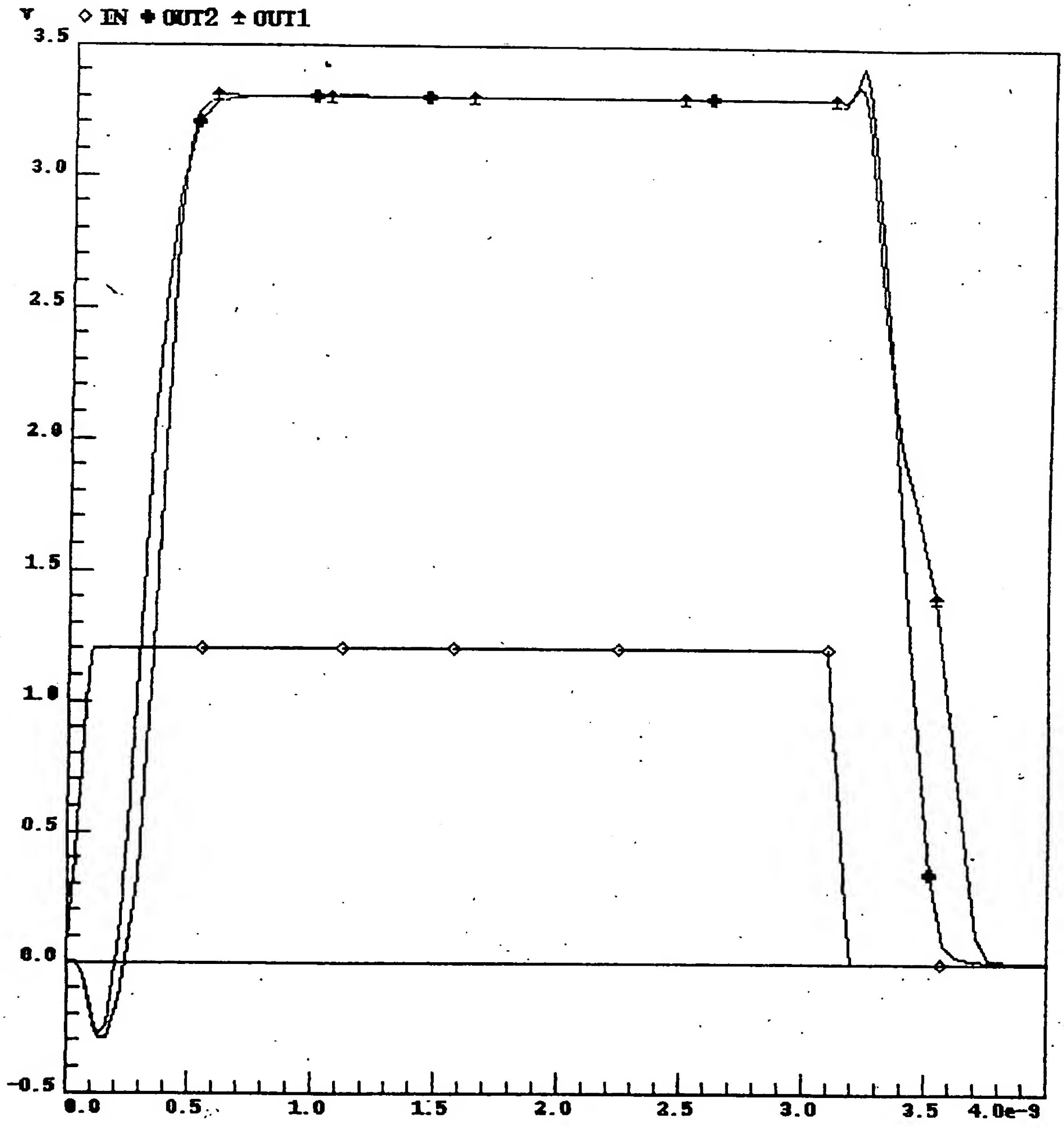

Fig. 5

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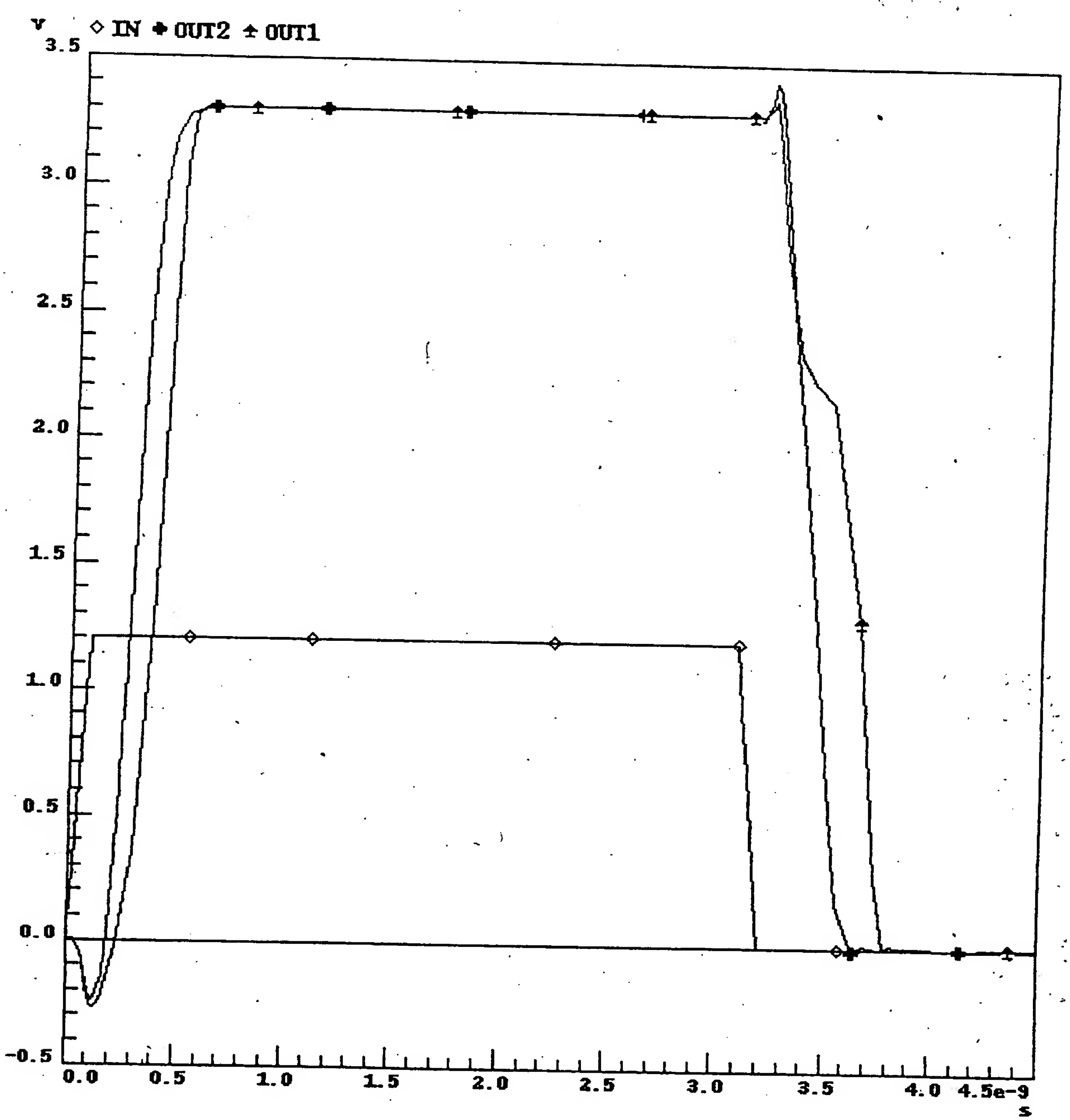

Fig. 6

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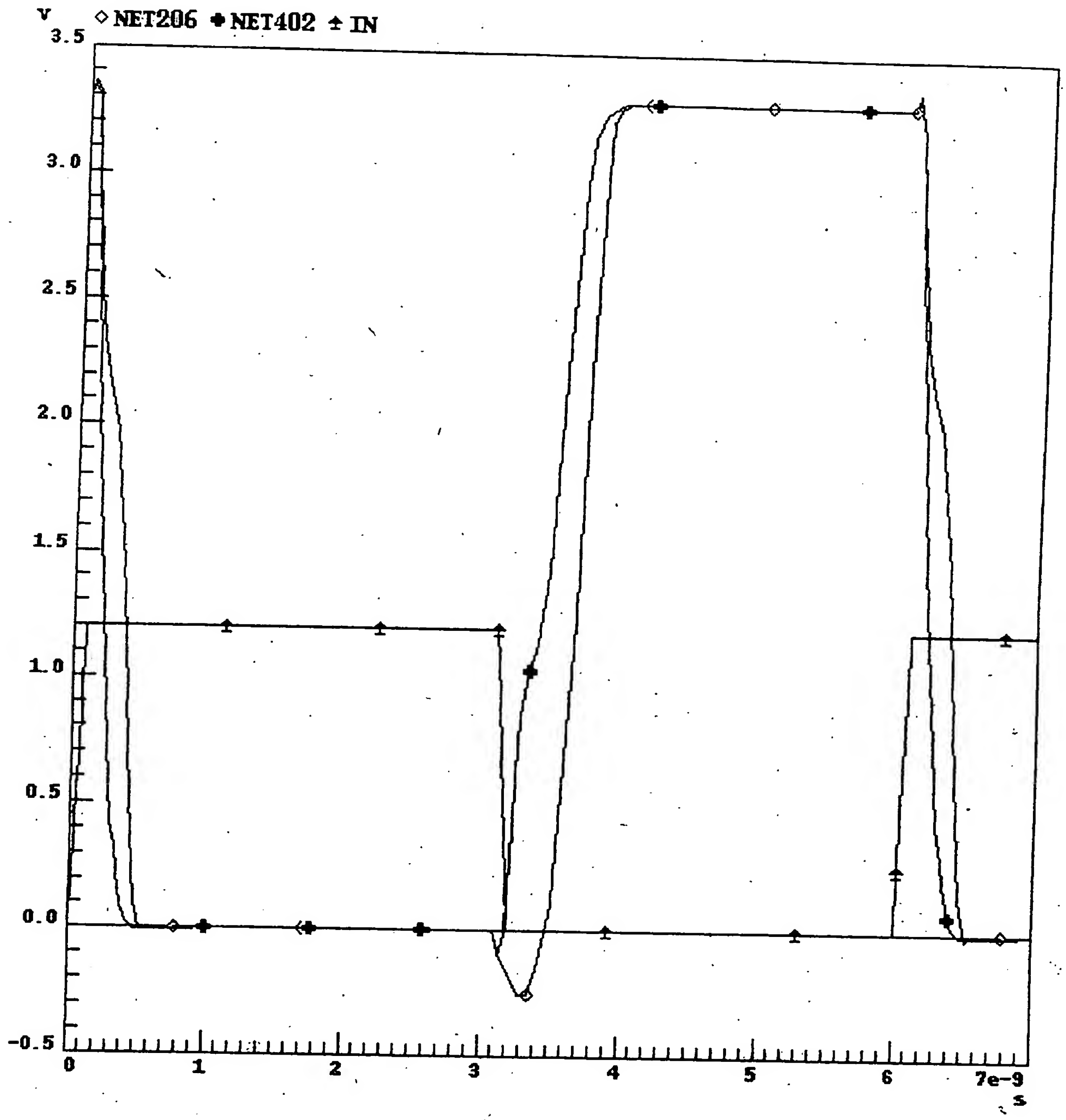

Fig. 7

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